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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LIU, MING HUN	
ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,677	KUDO ET AL.	
	Examiner	Art Unit	
	Ming-Hun Liu	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,34 and 36-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,34 and 36-38* is/are rejected.

7)☒ Claim(s) *39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. In the examiner initiated interview on 4/7/2005 to Robert Colwell, an agreement was reached regarding the grouping of the claimed invention. In order to expedite the prosecution of the application, the examiner will review the claims that belong to group I - claims 1-7, 34, and 36-40. Claims 19-24 and 35 have been withdrawn from consideration as they belong to separate groupings.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7, 34, 36 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,181,313 to Yokota et al.

In reference to claims 1 and 34, Yokota shows in figure 1 the hardware of his invention. The components that describe the method of claim 1 are elements OSC (oscillator), CPG (clock pulse generator) and Timing Generation Circuit (10). Yokota teaches a method that determines a reference clock period from a first number of original clock period (OSC) and determining the scanning period from a second number of said reference clock periods (ϕ) and changing the

scanning period by at least one reference clock period (column 6, lines 49-51 and column 8, lines 55-60). As for claim 34, it is inherent that the method be presented in computer program code.

In reference to claim 2, Yokota teaches a reference clock generator (CPG) for generating a reference clock period from a first number of original clock periods (OSC), a timing generator (timing generation circuit) coupled to reference clock generator for generating a line pulse synchronized with a scanning period (column 8, lines 55-64), with the scanning period having a second number of reference clock periods (ϕ) and a control register (common shift register, item 15) having a third number of reference clock periods (SCLK)for changing the scanning period, wherein the third number is at least one original clock period different from the second number (column 8, lines 50-60).

In reference to claim 3, Yokota teaches a controller and in figure 9, a control register (item 34) for storing operating parameters, comprising a first number of reference clock periods in a scanning period (column 8, lines 46-55; "adjusts the period of a shift clock signal SCLK") and a second number of scan lines in a frame period (column 3, lines 20-24). Yokota also teaches a reference clock generator (CPG) for generating reference clocks for a timing generator (timing generation circuit). The timing generator of Yokota is used for generating line pulses synchronized with one scanning period and frame pulses synchronized with one frame period (column 8, lines 50-60).

In reference to claim 4, Yokota teaches a controller where the operating parameters further comprise a division ratio ("frequency-dividing ratio" column 8, line 57) and wherein the reference clock from the reference generator is generated from an original clock using said division ratio.

In reference to claim 5, Yokota teaches a controller wherein the division ratio is one, as exhibited in figure 1, where the duty drive is 1/32.

In reference to claim 6, Yokota teaches a controller comprising an external computer coupled with the control register (MPU item 3) for determining the first number given the second number and a frame frequency (column 8, lines 43-60).

In reference to claim 7, Yokota teaches that the frequency-dividing ratio of the drive duty... is controlled based upon the drive duty value set (column 8, line 57-59).

In reference to claim 36, Yokota teaches a device for controlling a display panel, the device comprising, a first circuit for setting parameters for the display panel (item 5 - instruction register), a second circuit for generating a clock signal based on the parameters (item 10- timing generation circuit), and a third circuit for driving the display panel according to the clock signal (item 15- shift register).

In reference to claim 37, Yokota teaches a display control device for providing an adjustable scan frequency to a display panel, the display control device comprising a first circuit for setting a division ratio (timing generation circuit) of an original clock signal (OSC) and reference clock signal (CPG) based on information from an external device (MPU and column 8, lines 43-60). Yokota also teaches a second circuit for dividing the original clock signal by the division ratio to determine a frame frequency based thereon ("frequency-dividing circuit"). And last, Yokota teaches a circuit for converting data from the external device into a driving voltage signal to be coupled to the display panel (item 4 – system interface; column 6, line 10).

In reference to claim 38, Yokota teaches a device for controlling a display on a display panel on which a plurality of data lines and a plurality of scanning lines are arranged in a matrix

(figures 1 and 5a), the device comprising a first generator for generating an original clock signal (OSC), a memory for storing display data received from an external device (item 7 - display data memory DDRAM), a register for setting a division ratio of the original clock signal and the reference clock signal per a scanning period and a number of active lines of the display panel (item 34 – drive duty selection register; column 8, lines 44-49). Yokota also teaches, a second generator (item 10 - timing generation circuit) for dividing the original clock signal by the division ratio (column 8, line 56) to generate the reference clock (ϕ), to thereby generate a line pulse synchronized with a scanning period and a frame pulse synchronized with a frame period (column 8, lines 50-55). Yokota also teaches a data line driver (item 14 - segment driver) for reading out display data from the memory according to the line pulse and the frame pulse, for converting the display data into a driving voltage to be provided to the display panel (column 6, lines 26-30).

Allowable Subject Matter

4. Claims 38 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 5,854,540 to Matsumoto et al.

US Patent 6,064,356 to Shigeta

US Patent 6,020,872 to Mizukata et al.

US Patent 6,831,617 to Miyauchi et al.

US Patent 6,014,126 to Nishihara

US Patent 6,304,242 to Onda.

US Patent 6,774,878 to Yoshida et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ming-Hun Liu whose telephone number is (571)272-7770. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ming-Hun Liu

DENNIS-DOON CHOW
PRIMARY EXAMINER